WHAT IS CLAIMED:

1. A method of forming a ferroelectric memory device comprising:

polishing an insulating layer on a plurality of ferroelectric capacitors with a silica slurry to reduce a height of the insulating layer above a surface of the plurality of ferroelectric capacitors so that the surface remains covered by a portion of the insulating layer; and

polishing the insulating layer further with a ceria slurry to further reduce the height of the insulating layer and to expose a polishing stop layer on the surface of the plurality of ferroelectric capacitors.

2. A method according to Claim 1 further comprising:

removing the polishing stop layer with an etch-back process using RF sputtering to expose an upper electrode of the plurality of ferroelectric capacitors.

3. A method according to Claim 1 wherein polishing the insulating layer further with a ceria slurry comprises polishing the insulating layer with the ceria slurry at a faster rate than polishing the insulating layer with the silica slurry.

4. A method according to Claim 1 wherein the polishing stop layer comprises one of Al_2O_3, TiO_2, Ta_2O_5, $BaTiO_3$, $SrTiO_3$, $Bi_4Ti_3O_{12}$, and $PbTiO_3$.

5. A method of according to Claim 1 wherein the polishing stop layer comprises one of Si_3N_4 and SiON.

6. A method according to Claim 1 further comprising:

forming the polishing stop layer using plasma chemical vapor deposition.

7. A method according to Claim 1 wherein the insulating layer comprises one of undoped silicate glass, plasma enhanced oxide, high density plasma oxide, and phosphosilicate glass.

8. A method according to Claim 1 further comprising:

forming a plurality of conductive patterns directly on upper surfaces of at least one pair of adjacent ones of the plurality of ferroelectric capacitors.

9. A method according to Claim 1 wherein polishing an insulating layer on a plurality of ferroelectric capacitors with a silica slurry is preceded by:

forming a mask that covers the insulating layer on a peripheral circuit region of the ferroelectric memory device and exposes the insulating layer on a cell array region of the ferroelectric memory device; and

etching-back the insulating layer on the cell array region to a height that is less than a height of the insulating layer on peripheral circuit region, the method further comprising:

polishing the insulating layer on the plurality of ferroelectric capacitors with the silica slurry to reduce the height of the insulating layer on the cell array region;

removing the mask from the insulating layer on the peripheral circuit region; and

polishing the insulating layer on the cell array region and on the peripheral circuit region with the ceria slurry to expose the polishing stop layer and to reduce a step difference between respective height of the insulating layer on the cell array region and on the peripheral circuit region.

10. A method of manufacturing a ferroelectric memory device, the method comprising:

forming a plurality of ferroelectric capacitors in a cell array region on a substrate;

forming a barrier layer to cover ferroelectric capacitors in the cell array region and on the peripheral circuit region;

forming a polishing stop layer on the cell array region and on the peripheral circuit region to cover the barrier layer;

forming an insulating layer on the cell array region and on the peripheral circuit region to cover the polishing stop layer;

removing a portion of the insulating layer only in the cell array region to provide a first insulating pattern having a height above a surface ferroelectric capacitors in the cell array region;

planarizing the first insulating pattern in the cell array region and the peripheral circuit region using chemical mechanical polishing to form a planarized second insulating pattern that exposes the polishing stop layer; and

removing the exposed portion of the polishing stop layer and the barrier layer disposed thereunder until the top surface of the ferroelectric capacitor is exposed.

11. A method according to Claim 10, wherein removing a portion of the insulating layer only in the cell array region comprises selectively removing the portion of the insulating layer only in the cell array region by an etchback process using RF sputtering.

12. A method according to Claim 10 wherein the barrier layer comprises one of Al_2O_3, TiO_2, Ta_2O_5, $BaTiO_3$, $SrTiO_3$, $Bi_4Ti_3O_{12}$, and $PbTiO_3$.

13. A method according to Claim 10 wherein the polishing stop layer comprises one of Si_3N_4 and SiON.

14. A method according to Claim 10 wherein the insulating layer comprises one of undoped silicate glass, plasma enhanced oxide, high density plasma oxide, and phosphosilicate glass.

15. A method according to Claim 10 wherein planarizing the first insulating pattern in the cell array region and the peripheral circuit region comprises polishing the oxide layer using ceria slurry.

16. A method according to Claim 10 wherein planarizing the first insulating pattern in the cell array region and the peripheral circuit region using chemical mechanical polishing comprises polishing the insulating layer with the ceria slurry at a faster rate than polishing the insulating layer with the silica slurry.

17. A ferroelectric memory device comprising:

an oxide layer in a gap between adjacent ferroelectric memory capacitors on a substrate;

a barrier layer on sidewalls of the adjacent ferroelectric memory capacitors; and

a polishing stop layer between the barrier layer and the oxide layer comprising a material having an etch selectivity with respect to a slurry used for polishing the oxide layer, the etch selectivity of the slurry for the polishing stop layer being lower than that of the oxide layer.

18. A ferroelectric memory device according to Claim 17 wherein the polishing stop layer comprises of one of Si_3N_4 and SiON.

19. A ferroelectric memory device according to Claim 17 wherein the barrier layer comprises one of Al_2O_3, TiO_2, Ta_2O_5, $BaTiO_3$, $SrTiO_3$, $Bi_4Ti_3O_{12}$, and $PbTiO_3$.

20. A ferroelectric memory device according to Claim 17 wherein the oxide layer comprises one of undoped silicate glass, plasma enhanced oxide, high density plasma oxide, and phosphosilicate glass.

21. A ferroelectric memory device according to Claim 17 further comprising:

a buffer layer between the polishing stop layer and the oxide layer to improve an affinity of the oxide layer for the polishing stop layer.

22. A ferroelectric memory device according to Claim 21 wherein the buffer layer comprises one of Al_2O_3 and TiO_2.